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Digital Circuit Testing and Testability (The Morgan Kaufmann Series in Computer Architecture and Design)

Parag K. Lala

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In the past few years, reliable hardware system design has become increasingly important in the computer industry. **Digital Circuit Testing and Testability** is an easy to use introduction to the practices and techniques in this field.
Parag K. Lala writes in a user-friendly and tutorial style, making the book easy to read, even for the newcomer to fault-tolerant system design. Each informative chapter is self-contained, with little or no previous knowledge of a topic assumed. Extensive references follow each chapter, making further research in a particular area readily available. Each chapter covers a different aspect or technological component of fault-tolerant system design, and this book is an excellent compilation of up-to-date information in an area where such a book is needed.

Key Features
* Contains the most up-to-date information on fault modeling in CMOS devices
* Provides comprehensive coverage of self-checking logic design at the gate and the transistor level
* Discusses the latest techniques available for testing state machines
* Presents a collection of methods for testable logic synthesis
* Provides state-of-the-art information on Built-in-self-testing
* Includes detailed coverage of memory testing
* Discusses all major techniques for fault-tolerant hardware design

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